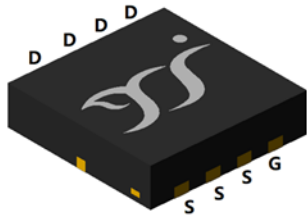
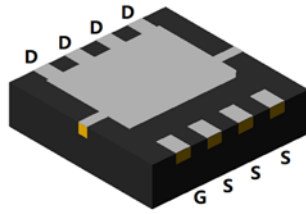


P-Channel Enhancement Mode Field Effect Transistor

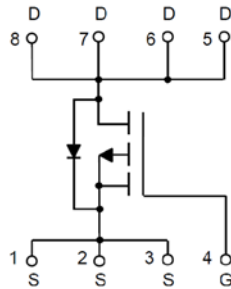


Top View



Bottom View

DFN3333-8L



Product Summary

- VDS -100V
- ID -16A
- RDS(ON)(at VGS=-10V) <85mΩ
- RDS(ON)(at VGS=-4.5V) <102mΩ
- 100% EAS Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low RDS(ON)
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit		
Drain-source Voltage	$T_J \geq 25^\circ\text{C}; T_J \leq 150^\circ\text{C}$		V_{DS}	-	-100	V		
Gate-source Voltage	$T_J \leq 150^\circ\text{C}; \text{DC}$		V_{GS}	-20	20			
Continuous Drain Current (Note 1,2)	Steady-State	$T_A = 25^\circ\text{C}, V_{GS} = -10\text{V}$	I_D	-	-3.3	A		
		$T_A = 100^\circ\text{C}, V_{GS} = -10\text{V}$		-	-2			
Continuous Drain Current (Note 1,3)	Steady-State	$T_C = 25^\circ\text{C}, V_{GS} = -10\text{V}, \text{Chip limitation}$		-	-16			
		$T_C = 100^\circ\text{C}, V_{GS} = -10\text{V}$		-	-10			
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p \leq 10\mu\text{s}$			I_{DM}	-		-60	
Maximum Body-Diode Continuous Current	$T_C = 25^\circ\text{C}$		I_S	-	-16			
Avalanche energy (non-repetitive)	$T_J = 25^\circ\text{C}, V_G = -10\text{V}, R_G = 25\Omega, L = 0.5\text{mH}, I_{AS} = -16\text{A}$		EAS	-	64	mJ		
Total Power Dissipation (Note 1,2)	Steady-State	$T_A = 25^\circ\text{C}$	P_D	-	1.92	W		
		$T_A = 100^\circ\text{C}$		-	0.76			
Total Power Dissipation (Note 1,3)	Steady-State	$T_C = 25^\circ\text{C}$		-	56			
		$T_C = 100^\circ\text{C}$		-	22			
Junction and Storage Temperature Range				T_J, T_{STG}	-55		150	$^\circ\text{C}$

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	65	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	2.2	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ085P10B	F1	Q085P10B	5000	10000	100000	13" reel



YJQ085P10B

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A, T_j=25^\circ C$	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-100V, V_{GS}=0V, T_j=25^\circ C$	-	-	-1	μA
		$V_{DS}=-100V, V_{GS}=0V, T_j=150^\circ C$	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V, T_j=25^\circ C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A, T_j=25^\circ C$	-1.5	-2	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A, T_j=25^\circ C$	-	66	85	$m\Omega$
		$V_{GS}=-4.5V, I_D=-5A, T_j=25^\circ C$	-	74	102	$m\Omega$
Diode Forward Voltage	V_{SD}	$I_S=-10A, V_{GS}=0V, T_j=25^\circ C$	-	-0.83	-1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^\circ C$	-	11.5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-50V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	2040	-	pF
Output Capacitance	C_{oss}		-	90	-	
Reverse Transfer Capacitance	C_{rss}		-	70	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-50V, I_D=-10A, T_j=25^\circ C$	-	44.4	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	
Gate-Drain Charge	Q_{gd}		-	5.5	-	
Reverse Recovery Charge	Q_{rr}	$I_F=-10A, di/dt=100A/\mu s, V_{GS}=0V, V_R=-15V, T_j=25^\circ C$	-	45	-	nC
Reverse Recovery Time	t_{rr}		-	30	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-50V, I_D=-10A, R_L=5\Omega, R_{GEN}=3\Omega, T_j=25^\circ C$	-	9	-	ns
Turn-on Rise Time	t_r		-	42	-	
Turn-off Delay Time	$t_{D(off)}$		-	91	-	
Turn-off fall Time	t_f		-	31	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of 150 $^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad)



Typical Electrical and Thermal Characteristics Diagrams

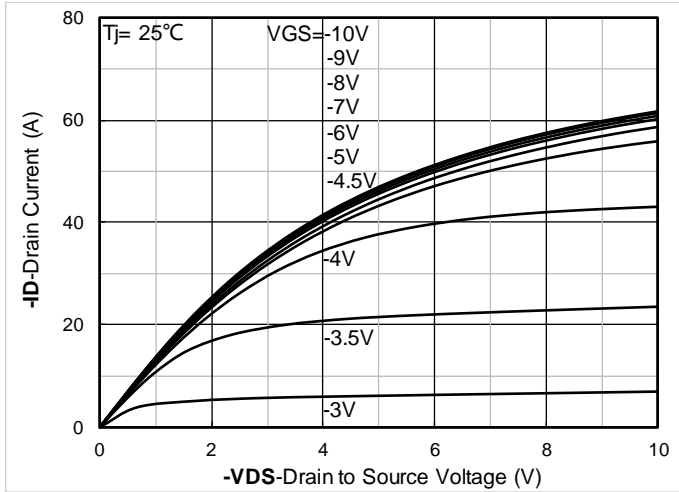


Figure 1. Output Characteristics; typical values

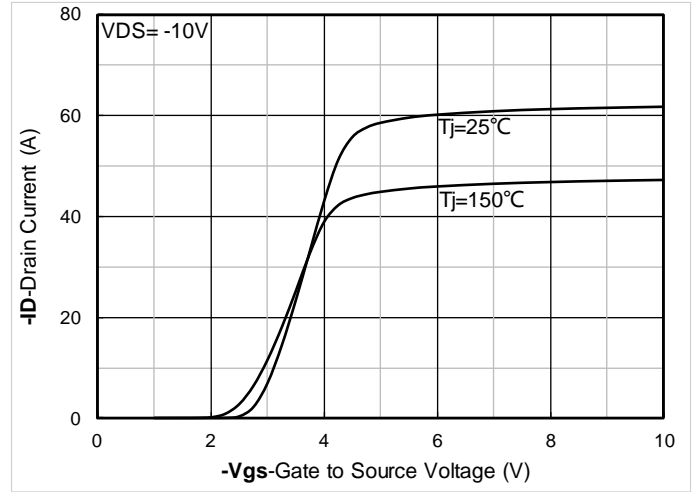


Figure 2. Transfer Characteristics; typical values

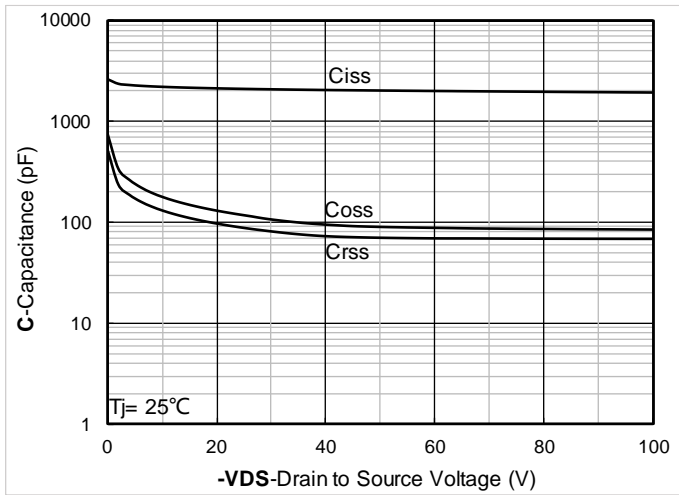


Figure 3. Capacitance Characteristics; typical values

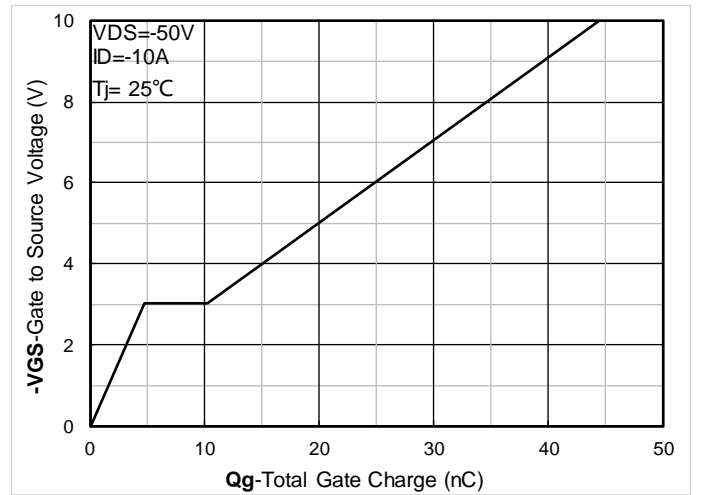


Figure 4. Gate Charge; typical values

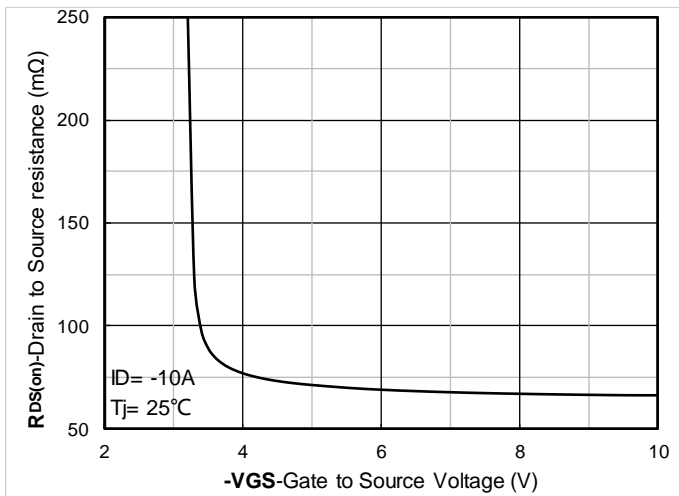


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

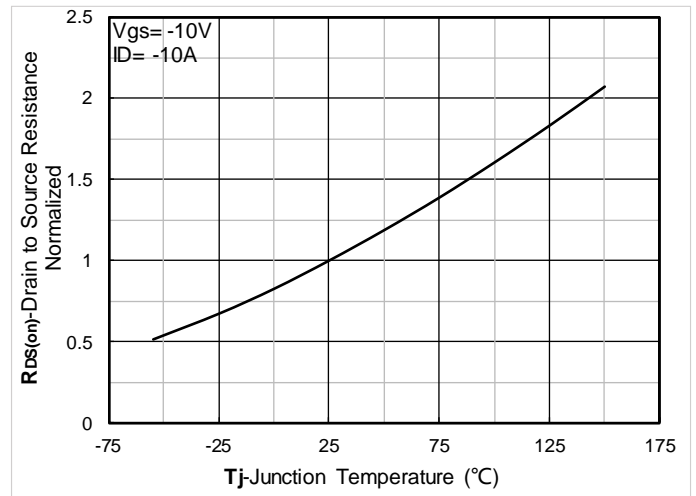


Figure 6. Normalized On-Resistance



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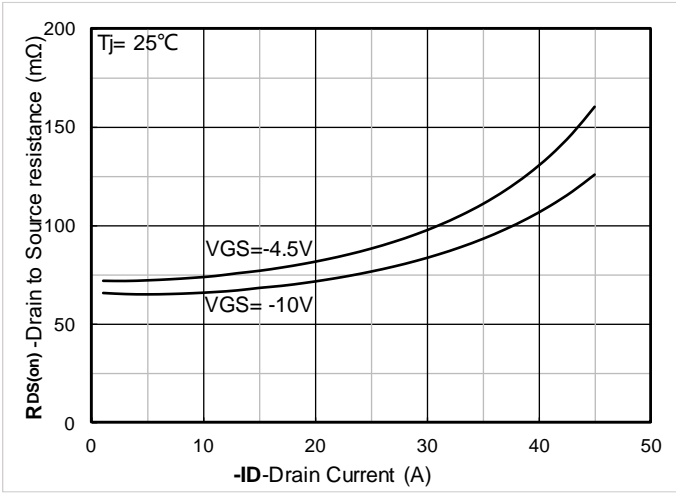


Figure 7. RDS(on) VS Drain Current; typical values

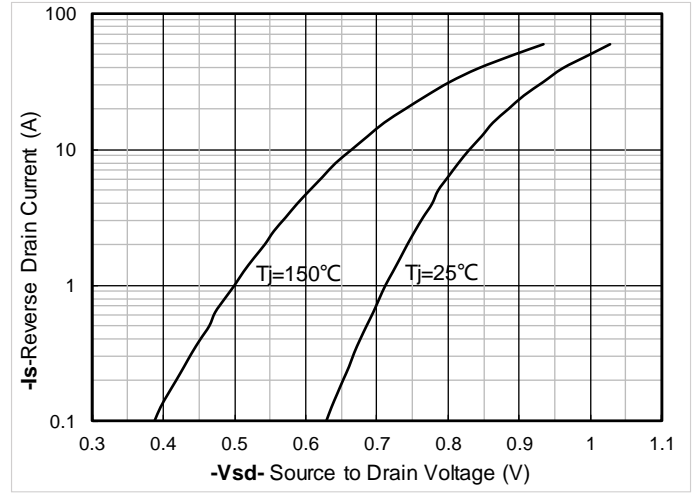


Figure 8. Forward characteristics of reverse diode; typical values

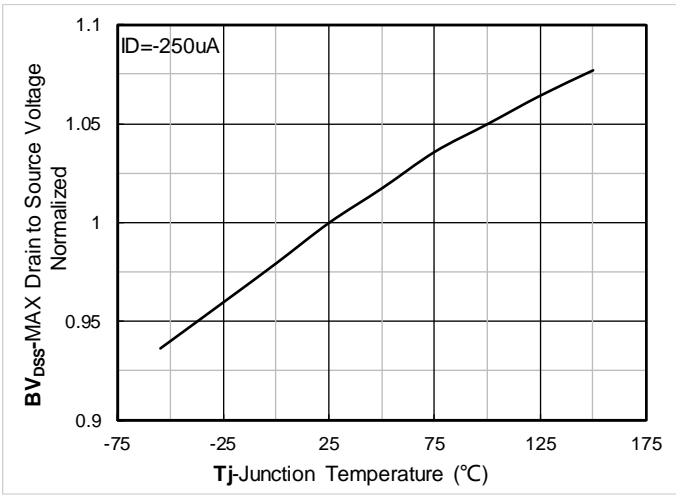


Figure 9. Normalized breakdown voltage

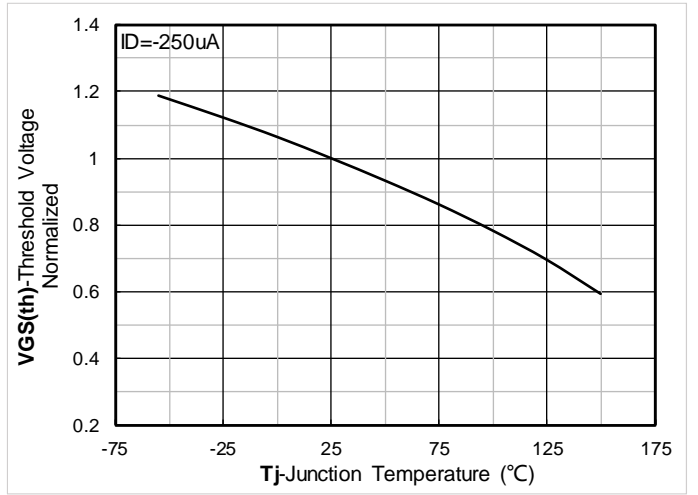


Figure 10. Normalized Threshold voltage

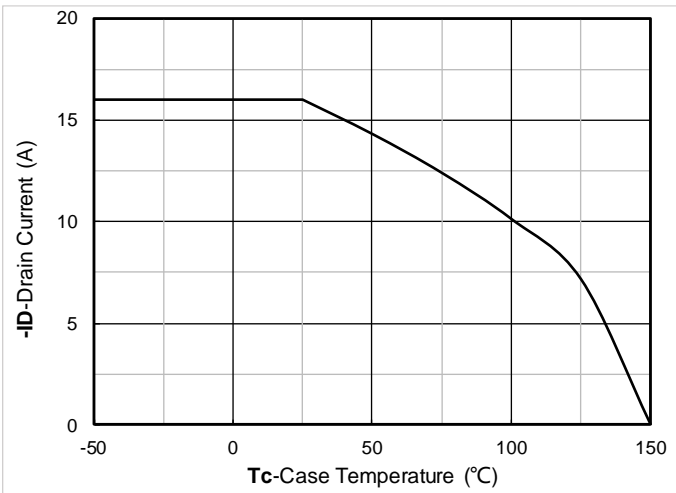


Figure 11. Current dissipation

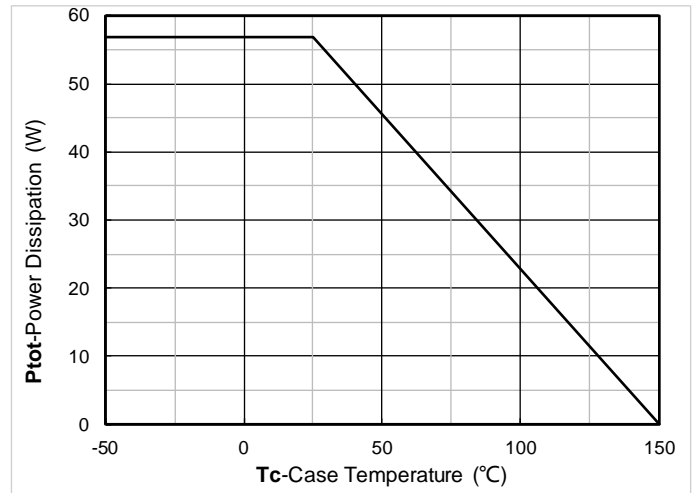


Figure 12. Power dissipation



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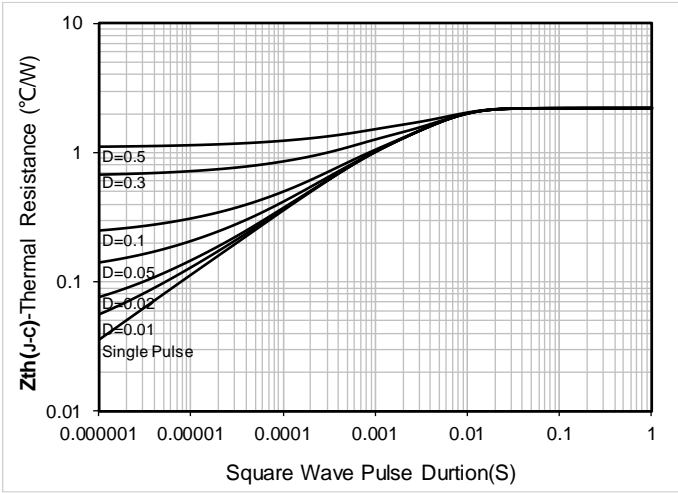


Figure 13. Maximum Transient Thermal Impedance

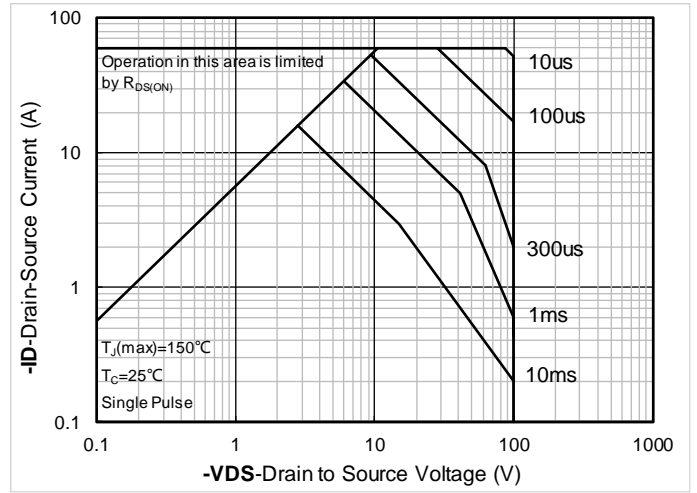
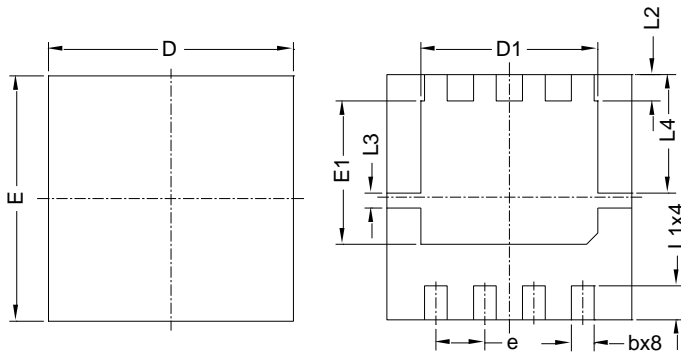


Figure 14. Safe Operation Area



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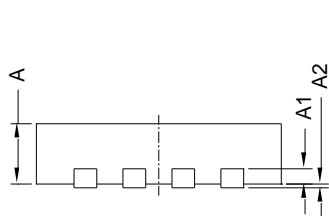
■ DFN3333-8L-A-0.8MM Package information



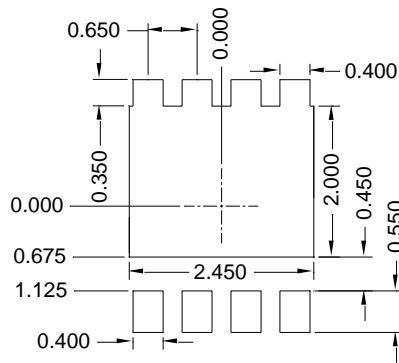
Top View
正面视图

Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
L3	0.20 BSC		
L4	1.57 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Side View
侧面视图



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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